

REMARKS

Claims 1-73 are pending in the application. Claims 3-6, 11, 12, 17, and 65-67 are allowed. Claims 1, 2, 7-10, 13-16, 18-64, and 68-73 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over various combinations of U.S. Patent Number 6,236,064 to Mase et al. ("Mase"), U.S. Patent Number 5,403,772 to Zhang et al. ("Zhang"), and U.S. Patent Number 5,585,658 to Mukai et al. ("Mukai").

In view of the amendments and following remarks, Applicants respectfully traverse the rejections.

Claim 1

Claim 1 is patentable over the references at least because neither Mase, Mukai, nor Zhang teaches or suggests that "said impurity regions have a total width of W_{pi} in a direction of a channel width W , and a total width of said intrinsic or substantially intrinsic region is W_{pa} in said direction of said channel width W , where $W_{pi}/W = 0.1$ to 0.9 and $W_{pa}/W = 0.1$ to 0.9 ," as recited in claim 1.

The Office Action alleges on page 5 that it is well known in the art to space regions into intervals wherein there are could be 1 to 9 regions and 1 to 9 intervals between the regions in the direction of a channel width, and that would mean that

impurity regions can have a total width of W_{pi} in a direction of a width W , and a total of the intervals in W_{pa} in a direction of the width, wherein $W_{pi}/W = 0.1$ to 0.9 and $W_{pa}/W = 0.1$ to 0.9 . The Office Action further alleges that it would have been obvious to one of ordinary skill in the art at the time of the present invention to use spacing of the intervals in an orderly manner such as 1 to 9 impurity regions and 1 to 9 interval in the method of Mase in order to have a set pattern which can be formed in a grid like fashion.

However, neither Mase, Mukai, nor Zhang teaches or suggests that said impurity regions have a total width of W_{pi} in a direction of a channel width W , and a total width of said intrinsic or substantially intrinsic region is W_{pa} in said direction of said channel width W , where $W_{pi}/W = 0.1$ to 0.9 and $W_{pa}/W = 0.1$ to 0.9 .

The motivation to provide such relationships between W , W_{pi} , and W_{pa} is found on page 31 of Applicants' specification. Although the motivation offered by the Examiner--that "it would have been obvious to one of ordinary skill in the art at the time of the present invention to use spacing of the intervals in an orderly manner such as 1 to 9 impurity regions and 1 to 9 interval in the method of Mase in order to have a set pattern which can be formed in a grid like fashion"-- may possibly be

motivation to provide some relationship between the above widths, Applicants respectfully assert that it is not motivation to provide the particular claimed relationships. The office action fails to point to any motivation to provide these particular claimed relationships.

At least because none of the references teaches or suggests this aspect of claim 1, and because there is no motivation to provide this aspect, claim 1 is patentable over the references, alone or in combination.

Claims 2 and 68

Claims 2 and 68 depend from claim 1 and are therefore patentable for at least the same reasons as stated above with respect to claim 1.

Claim 7

Claim 7 has been amended to recite "forming an intrinsic or substantially intrinsic region and an oxide region in said part to become the channel forming region by thermally treating said crystal semiconductor comprising silicon at a temperature of 1000 °C or higher to change a region of said crystal semiconductor implanted with said oxygen ion by said implanting step into said oxide."

Claim 7 is patentable over Mase and Zhang at least because the references neither teach or suggest that the thermal treatment is conducted at a temperature of 1000 °C or higher.

Claims 8 and 69

Claims 8 and 69 depend from claim 7 and are therefore patentable for at least the same reasons as stated above with respect to claim 7.

Claim 9

Claim 9 has been amended to recite that "said impurity regions have a total width of W_{pi} in a direction of a channel width W , and a total width of said intrinsic or substantially intrinsic region is W_{pa} in said direction of said channel width W , where $W_{pi}/W = 0.1$ to 0.9 and $W_{pa}/W = 0.1$ to 0.9 ."

As stated above with respect to claim 1, neither Mase, Mukai, nor Zhang teach this feature of claim 9, and therefore claim 9 is patentable for at least this reason.

Claims 10 and 70

Claims 10 and 70 depend from claim 9 and are therefore patentable for at least the same reasons as stated above with respect to claim 9.

Claim 13

Claim 13 recites that "said impurity regions have a total width of W_{pi} in a direction of said channel width W , and a total

width of said intrinsic or substantially intrinsic region is W_{pa} in said direction of said channel width W , where $W_{pi}/W = 0.1$ to 0.9 and $W_{pa}/W = 0.1$ to 0.9 ," and is therefore patentable for at least the same reasons as stated above with respect to claim 1.

Claims 14 and 71

Claims 14 and 71 depend from claim 13 and are therefore patentable for at least the same reasons as stated above with respect to claim 13.

Claim 15

Claim 15 has been amended to recite that "said impurity regions have a total width of W_{pi} in a direction of a channel width W , and a total width of said intrinsic or substantially intrinsic region is W_{pa} in said direction of said channel width W , where $W_{pi}/W = 0.1$ to 0.9 and $W_{pa}/W = 0.1$ to 0.9 ," and is therefore patentable for at least the same reasons as stated above with respect to claim 1.

Claims 16 and 72

Claims 16 and 72 depend from claim 15 and are therefore patentable for at least the same reasons as stated above with respect to claim 15.

Claim 18

Claim 18 is patentable over Mase and Zhang at least because neither reference teaches or suggests "wherein said impurity

region formed in said channel forming region pins a depletion layer that expands from said drain region toward said channel forming region and said source region," as recited in claim 18.

In Column 5, Mase discloses that it is advantageous to implant oxygen, carbon, or nitrogen ions into only parts of the channel formation regions of the TFTs forming pixels at a dopant concentration of 5×10^{19} to 5×10^{21} ions/cm³ so that the sensitivity to light may drop. The reference to Mase does not suggest that oxygen, carbon, or nitrogen ions are implanted into only parts of the channel formation regions in order to pin a depletion layer, as recited in claim 18. Reducing the sensitivity to light is not the same as pinning a depletion layer. Therefore, Mase does not teach this aspect of claim 18. Since Zhang does not remedy the deficiency of Mase, claim 18 is patentable over the references, alone or in combination.

Claims 24-29 and 73

Claims 24-29 and 73 depend from claim 18 and are therefore patentable for at least the same reasons as stated above with respect to claim 18.

Claim 19

Claim 19 is patentable over Mase and Zhang at least because neither reference teaches or suggests that "said impurity region

controls the threshold voltage to a predetermined value voltage," as recited in claim 19.

The reference to Mase discloses in column 5 that it is advantageous to implant oxygen, carbon, or nitrogen ions into only parts of the channel formation regions of the TFTs forming pixels at a dopant concentration of 5×10^{19} to 5×10^{21} ions/cm³ so that the sensitivity to light may drop. The reference to Mase does not suggest that oxygen, carbon, or nitrogen ions are implanted into only parts of the channel formation regions in order to control the threshold voltage to a predetermined value voltage. Since to drop the sensitivity to light is not to control the threshold voltage to a predetermined value voltage, Mase does not teach or suggest this aspect of claim 19. Zhang does not remedy the deficiency of Mase, and so claim 19 is patentable over the references, alone or in combination.

Claims 30-36

Claims 30-36 depend from claim 19, and are therefore patentable for at least the same reasons stated above with respect to claim 19.

Claim 20

Claim 20 has been amended to recite that "said impurity regions have a total width of W_{pi} in a direction of a channel width W , and a total width of said intrinsic or substantially

intrinsic region is Wpa in said direction of said channel width W, where $W_{pi}/W = 0.1$ to 0.9 and $W_{pa}/W = 0.1$ to 0.9 ," and is therefore patentable for at least the same reasons as stated above with respect to claim 1.

Claims 37-43

Claims 37-43 depend from claim 20, and are therefore patentable for at least the same reasons stated above with respect to claim 20.

Claim 21

Claim 21 is patentable over Mase and Zhang at least because neither reference teaches or suggests "wherein said impurity region pins a depletion layer that expands from said drain region toward said channel forming region and said source region," as recited in claim 21.

As stated above with respect to claim 18, in Column 5, Mase discloses that it is advantageous to implant oxygen, carbon, or nitrogen ions into only parts of the channel formation regions of the TFTs forming pixels at a dopant concentration of 5×10^{19} to 5×10^{21} ions/cm³ so that the sensitivity to light may drop. The reference to Mase does not suggest that oxygen, carbon, or nitrogen ions are implanted into only parts of the channel formation regions in order to pin a depletion layer, as recited in claim 18. Reducing the sensitivity to light is not the same

as pinning a depletion layer. Therefore, Mase does not teach this aspect of claim 21. Since Zhang does not remedy the deficiency of Mase, claim 21 is patentable over the references, alone or in combination.

Claims 44-50

Claims 44-50 depend from claim 21, and are therefore patentable for at least the same reasons stated above with respect to claim 21.

Claim 22

Claim 22 is patentable over Mase and Zhang at least because neither reference teaches or suggests that "said impurity region controls the threshold voltage to a predetermined value voltage," as recited in claim 22.

As stated above with respect to claim 19, the reference to Mase discloses in column 5 that it is advantageous to implant oxygen, carbon, or nitrogen ions into only parts of the channel formation regions of the TFTs forming pixels at a dopant concentration of 5×10^{19} to 5×10^{21} ions/cm³ so that the sensitivity to light may drop. The reference to Mase does not suggest that oxygen, carbon, or nitrogen ions are implanted into only parts of the channel formation regions in order to control the threshold voltage to a predetermined value voltage. Since to drop the sensitivity to light is not to control the threshold

voltage to a predetermined value voltage, Mase does not teach or suggest this aspect of claim 22. Zhang does not remedy the deficiency of Mase, and so claim 22 is patentable over the references, alone or in combination.

Claims 51-57

Claims 51-57 depend from claim 22, and are therefore patentable for at least the same reasons stated above with respect to claim 22.

Claim 23

Claim 23 has been amended to recite that "said impurity regions have a total width of W_{pi} in a direction of a channel width W , and a total width of said intrinsic or substantially intrinsic region is W_{pa} in said direction of said channel width W , where $W_{pi}/W = 0.1$ to 0.9 and $W_{pa}/W = 0.1$ to 0.9 ," and is therefore patentable for at least the same reasons as stated above with respect to claim 1.

Claims 51-64

Claims 51-64 depend from claim 23, and are therefore patentable for at least the same reasons stated above with respect to claim 23.

Allowed subject matter

Applicants acknowledge and thank the Examiner for the indication of allowability of claims 3-6, 11, 12, 17, and 65-67.

Attached is a marked-up version of the changes being made by the current amendment.

CONCLUSION

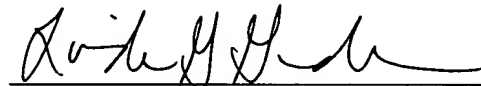
In view of the above amendments and remarks, Applicants believe that claims 1-73 are in condition for allowance, and request a notice of allowance.

Enclosed is a \$400 check for the Petition for Extension of Time fee. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: _____

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Version with markings to show changes made

In the claims:

Claims 1, 7, 9, 15, 20, and 23 have been amended as follows:

1. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising [the steps of]:

forming a resist over a crystal semiconductor comprising a part to become a channel forming region;

forming a dotted hole in said resist by patterning said resist using electron drawing method or FIB method;

forming an intrinsic or substantially intrinsic region and an impurity region in said part to become the channel forming region by introducing a first impurity into said impurity region through said resist having said dotted hole, said first impurity being selected from the group consisting of carbon, nitrogen and oxygen; and

introducing into said crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween,

wherein [a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity region formed in said part to become the channel

forming region] said impurity regions have a total width of W_{pi} in a direction of a channel width W , and a total width of said intrinsic or substantially intrinsic region is W_{pa} in said direction of said channel width W , where $W_{pi}/W = 0.1$ to 0.9 and $W_{pa}/W = 0.1$ to 0.9 .

7. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising [the steps of]:

implanting an oxygen ion into a crystal semiconductor comprising a part to become a channel forming region by a convergent ion beam or an electron beam, said crystal semiconductor comprising silicon;

forming an intrinsic or substantially intrinsic region and an oxide region in said part to become the channel forming region by thermally treating said crystal semiconductor comprising silicon at a temperature of 1000°C or higher to change a region of said crystal semiconductor implanted with said oxygen ion by said implanting step into said oxide; and

introducing into said crystal semiconductor an impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween[,

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said oxide region formed in said part to become the channel forming region].

9. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising [the steps of]:

forming an intrinsic or substantially intrinsic region and an impurity region in a part of a crystal semiconductor to become a channel forming region by introducing a first impurity into said impurity region, said impurity region containing an element selected from the group consisting of carbon, nitrogen and oxygen as said first impurity; and

introducing into said crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween,

wherein [a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity region formed in said part to become the channel forming region] said impurity regions have a total width of W_{pi} in a direction of a channel width W , and a total width of said intrinsic or substantially intrinsic region is W_{pa} in said

direction of said channel width W, where $W_{pi}/W = 0.1$ to 0.9 and $W_{pa}/W = 0.1$ to 0.9 .

15. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising [the steps of]:

forming a resist over a crystal semiconductor comprising a part to become a channel forming region;

forming a dotted hole in said resist by patterning said resist using electron drawing method or FIB method;

forming an intrinsic or substantially intrinsic region and a plurality of impurity regions in said part to become the channel forming region by introducing a first impurity into said impurity regions through said resist having said dotted hole, said first impurity being selected from the group consisting of carbon, nitrogen and oxygen; and

introducing into said crystal semiconductor a second impurity that gives one conductivity to form a source region and a drain region in said crystal semiconductor with said channel forming region therebetween,

wherein said impurity regions form one or a plurality of rows extending in a direction of a channel length of said channel forming region, and

wherein [a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity regions formed in said part to become the channel forming region] said impurity regions have a total width of W_{pi} in a direction of a channel width W , and a total width of said intrinsic or substantially intrinsic region is W_{pa} in said direction of said channel width W , where $W_{pi}/W = 0.1$ to 0.9 and $W_{pa}/W = 0.1$ to 0.9 .

20. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising [the steps of]:

forming a source region, a drain region and a channel forming region using a crystal semiconductor;

forming an intrinsic or substantially intrinsic region and an impurity region in said channel forming region; and

forming a gate insulating film and a gate electrode over said channel forming region,

wherein an impurity element that expand an energy band width (E_g) is added to said impurity region[, and

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity region formed in said channel forming region], and

wherein said impurity regions have a total width of W_{pi} in a direction of a channel width W , and a total width of said intrinsic or substantially intrinsic region is W_{pa} in said direction of said channel width W , where $W_{pi}/W = 0.1$ to 0.9 and $W_{pa}/W = 0.1$ to 0.9 .

23. (Amended) A method of manufacturing an insulated gate semiconductor device, said method comprising [the steps of]:

forming a source region, a drain region and a channel forming region using a crystal semiconductor; and

forming an intrinsic or substantially intrinsic region and an impurity region in said channel forming region; and

forming a gate insulating film and a gate electrode over said channel forming region,

wherein said impurity region has an insulating property, wherein an impurity element that expands an energy band width (E_g) is added to said impurity region[, and

wherein a carrier moves through said intrinsic or substantially intrinsic region while said carrier avoids said impurity region formed in said channel forming region], and

wherein said impurity regions have a total width of W_{pi} in a direction of a channel width W , and a total width of said intrinsic or substantially intrinsic region is W_{pa} in said

direction of said channel width W, where $W_{pi}/W = 0.1$ to 0.9 and
 $W_{pa}/W = 0.1$ to 0.9 .